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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/836,065	04/16/2001	Janevoot Naksrikram	P1310	5713

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EXAMINER	
CHAUDRY, MUJTABA M	
ART UNIT	**PAPER NUMBER**
2133	8

DATE MAILED: 05/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/836,065	NAKSRIKRAM ET AL.	
	Examiner	Art Unit	
	Mujtaba K Chaudry	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☒ Claim(s) *1,3,8,10 and 17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because:

- Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g).
- Figure 1 does not show "sector 7" as indicated on page 3, line 28 of specification. Clarification and/or correction is requested.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities:

- Applicant is reminded of the proper language and format for an abstract of the disclosure.

  The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

  The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because the first sentence of the abstract is considered to be a "run-on" and therefore needs to be rewritten. Applicant is suggested to revise the abstract in accordance with the guidelines provided above. Correction is required. See MPEP § 608.01(b).

- On page 3, line 28 of specification "sector 7" does not appear in the Figure as indicated in the specification. Clarification and/or correction is requested.
- On page 6, the last sentence on lines 6-8 should be omitted because it does not seem appropriate for the specification.

Appropriate correction is required.

Claim Objections

Claims 1 and 10 are objected to because of the following informalities:

- In line 2, the limitations **"first sector of a first sector type"** and **"a second sector of a second sector type"** do not indicate what the first type and second type actually are. For example, Applicants are suggested to insert "memory" after "...type."

Appropriate correction is required.

Claim 3 is objected to because of the following informalities:

- The term **"APDE"** needs to be written out.
- In line 5, after **"APDE time periods"** and line 6, after **"third time periods"** Applicants are suggested to use **";"**

- In line 5, after **"at least one of"** and line 6, after **"at least one of"** Applicants are suggested to omit **":"**
- Applicants are requested to review other similar claims and make corrections as indicated hereinabove.

Appropriate correction is required.

Claim 10 is objected to because of the following informalities:

- In line 1, the phrase **"A system a semiconductor device..."** does not make grammatical sense. Applicants are advised to perhaps use **"A system including a semiconductor device..."**

Appropriate correction is required.

Claim 8 is objected to because of the following:

- Claim 8 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 8 fails to further limit the parent claim because the limitation of "executing at least one parameter test on the device" is well known in testing a semiconductor device.

Appropriate correction is required.

Claim 17 is objected to because of the following:

- Claim 17 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 17 fails to further limit the parent claim because the limitation of "executes at least one parameter test on the device" is well known in testing a semiconductor device.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

- Claim 2 recites the limitation "the device" in line 1. There is insufficient antecedent basis for this limitation in the claim. Applicants are suggested to use "semiconductor device" to avoid antecedent issues. As for examination purposes, the Examiner will assume such interpretation.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.

3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi (USPN 5343434) further in view of Kobayashi et al. (USPN 5646948).

As per claims 1 and 10, Noguchi substantially teaches (title and abstract) a method and apparatus for performing erase testing on a semiconductor device. Noguchi teaches a memory device in a bare chip state which is determined as fail by over erasing during a test at a wafer level, information indicating the presence of an over-erased memory cell is stored in a nonvolatile and readable manner into an identification memory circuit, and then memory cells in a memory cell array are restored to an erase state of an electrically neutral state by irradiation with an energy beam such as ultraviolet rays. A chip erased by the energy beam such as ultraviolet rays is assembled as an OTPROM (one-time programmable read only memory) and tested. At that time, a writing/erasing control circuit for controlling data writing into and data erasing in the memory cells is brought into an operation-inhibited state in accordance with the information stored in the memory circuit. It is possible to reduce the rate at which fail products are produced by use of a flash memory which is determined as fail because of the presence of an over-erased memory cell as a one-time programmable memory device. Furthermore, Noguchi teaches (Figure 14) the erasing operation of a nonvolatile semiconductor memory device. First, at the stage of initializing, a program high voltage Vpp is applied to the instruction port controller 2 to render the instruction port controller 2 operative (a step S2). Then, specific data (00H) is programmed for all bytes (data input/output is carried out in the units of byte and erasing is carried out also in the units of byte) (a step S4). This data programming is made in

order to bring each memory cell into a write state and set the threshold voltage of each memory cell to be substantially equal. The Examiner would like to point out that this step is analogous to establishing a first test limit as stated in the present application. In addition, each counter is preset to a predetermined initial value (a step S6). This counter includes a counter for counting the number of time CUMTEW of the increase of an erase pulse width TEW, and a counter for counting the number of times PLSCNT by which erase pulses are generated. An address is set to 0. Then, an erase setup instruction is written into the instruction port controller 2 (the status register 235 and the instruction register 237) (a step S8), and an erase instruction is subsequently written into the instruction port controller 2 (a step S10). An erasing with respect to all the memory cells is executed in accordance with the writing of the erase instruction (a step S12). After a predetermined time period has passed, it is determined that the erasing of the memory cells is completed, and an erase verify instruction is written into the instruction port controller 2 (the status register 235 and the instruction register 237) (a step S14). In accordance with this erase verify instruction, an erase verify voltage is generated from the erase/program verification generator 9 and then transmitted via the X decoder 12 onto a selected word line in the memory cell array (a step S16). When a predetermined time period has passed (time T2), data reading is carried out (a step S18). If the read data is an erased data, then the data is "1". If the read data is an unerased data, then the data is "0". A determination is made as to whether this data is in the erased state or not in accordance with its value (a step S20). If the data indicates the unerased state, then an erase pulse width to be applied to erase the data is incremented by a predetermined value, and this incremented erase pulse width information is stored in the TEW counter (a

step S22). A determination is first made as to whether the erase pulse width stored in the TEW counter reaches a maximum limit value, and subsequently, a determination is made as to whether the number by which the erase pulses are applied reaches a predetermined value (64 times) (a step S24). When the erase pulse application number PLSCNT reaches the predetermined value (64 times), it is determined that no erasing is allowed for that memory cell any more, and an erase error is stored (a step S26). When the erase pulse application number PLSCNT does not reach the predetermined value in the step S24, the processing returns to the step S8, in which the writing and erasing operation by the erase setup instruction and the erase instruction is carried out.

Noguchi does not explicitly teach to have a first sector of a first sector type and a second sector with a second sector type as stated in the present application.

However, Kobayashi et al. (herein after: Kobayashi), in an analogous art, substantially teaches (title and abstract) a method and apparatus for testing a plurality of semiconductor memories in parallel. Kobayashi teaches a test data pattern, an address pattern, and a control signal are supplied from a pattern generator to a test memory. Data read from the test memory is compared with expected data by an XOR gate. When they match, a compared result that represents pass is output. When they mismatch, a compared result that represents fail is output. A match signal WC detected by the XOR gate is held in a register. The register outputs an inhibition signal to an inhibition gate of the test memory. Thus, a write enable signal WE is inhibited from being supplied to the test memory. In addition, the inhibition signal is supplied to a compared result inhibition gate. The compared result inhibition gate causes the compared result to be passed and prevents the test memory from being excessively written. Therefore, it

would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the multiple memories of Kobayashi with the testing apparatus of Noguchi. This modification would have been obvious to one of ordinary skill in the art because one of ordinary skill in the art would have recognized that by applying the testing routine taught by Noguchi with multiple memory types would reduce overall testing time.

As per claims 2-6 and 11-15, Noguchi substantially teaches, in view of above rejections, (Figure 1) a block diagram showing an overall structure of a nonvolatile semiconductor memory device according to one embodiment. FIG. 1 shows a structure of a flash memory in which all memory cells in a memory cell array 13 are brought into an erase state at the same time. This structure corresponds to the structure of the conventional nonvolatile semiconductor memory device shown in FIG. 12. The structure of this memory device is applicable not only to the flash memory in which all memory cells of the memory cell array 13 are erased at the same time but also to a nonvolatile semiconductor memory device of the type in which erasing is made in units of a sector, a word line or a byte. Corresponding portions of the memory device of FIG. 1 to those of the conventional nonvolatile semiconductor memory device shown in FIG. 12 are denoted with the same reference numerals. Moreover, in an erasing operation, the same effects as those provided in the foregoing embodiment can be obtained even in a structure in which not every memory cell is erased at the same time but only memory cells to be programmed are erased. That is, the same effects as those provided in the foregoing embodiment can be obtained even in a nonvolatile semiconductor memory device in which data erasing is carried out in the units of word line, the units of byte or the units of sector. Furthermore, an erase setup instruction is written into the instruction port controller 2 (the status register 235 and the instruction register

237) (a step S8), and an erase instruction is subsequently written into the instruction port controller 2 (a step S10). An erasing with respect to all the memory cells is executed in accordance with the writing of the erase instruction (a step S12). After a predetermined time period has passed, it is determined that the erasing of the memory cells is completed, and an erase verify instruction is written into the instruction port controller 2 (the status register 235 and the instruction register 237) (a step S14). In accordance with this erase verify instruction, an erase verify voltage is generated from the erase/program verification generator 9 and then transmitted via the X decoder 12 onto a selected word line in the memory cell array (a step S16). When a predetermined time period has passed (time T2), data reading is carried out (a step S18).

As per claims 7-9 and 16-18, Noguchi substantially teaches, in view of above rejections, the erasing operation of a nonvolatile semiconductor memory device. First, at the stage of initializing, a program high voltage Vpp is applied to the instruction port controller 2 to render the instruction port controller 2 operative (a step S2). Then, specific data (00H) is programmed for all bytes (data input/output is carried out in the units of byte and erasing is carried out also in the units of byte) (a step S4). This data programming is made in order to bring each memory cell into a write state and set the threshold voltage of each memory cell to be substantially equal. The Examiner would like to point out that this step is analogous to establishing a first test limit as stated in the present application. In addition, each counter is preset to a predetermined initial value (a step S6). This counter includes a counter for counting the number of time CUMTEW of the increase of an erase pulse width TEW, and a counter for counting the number of times PLSCNT by which erase pulses are generated. An address is set to 0. Then, an erase setup instruction is written into the instruction port controller 2 (the status register 235 and the

instruction register 237) (a step S8), and an erase instruction is subsequently written into the instruction port controller 2 (a step S10). An erasing with respect to all the memory cells is executed in accordance with the writing of the erase instruction (a step S12). After a predetermined time period has passed, it is determined that the erasing of the memory cells is completed, and an erase verify instruction is written into the instruction port controller 2 (the status register 235 and the instruction register 237) (a step S14). In accordance with this erase verify instruction, an erase verify voltage is generated from the erase/program verification generator 9 and then transmitted via the X decoder 12 onto a selected word line in the memory cell array (a step S16). When a predetermined time period has passed (time T2), data reading is carried out (a step S18). If the read data is an erased data, then the data is "1". If the read data is an unerased data, then the data is "0". A determination is made as to whether this data is in the erased state or not in accordance with its value (a step S20). If the data indicates the unerased state, then an erase pulse width to be applied to erase the data is incremented by a predetermined value, and this incremented erase pulse width information is stored in the TEW counter (a step S22). A determination is first made as to whether the erase pulse width stored in the TEW counter reaches a maximum limit value, and subsequently, a determination is made as to whether the number by which the erase pulses are applied reaches a predetermined value (64 times) (a step S24). When the erase pulse application number PLSCNT reaches the predetermined value (64 times), it is determined that no erasing is allowed for that memory cell any more, and an erase error is stored (a step S26). When the erase pulse application number

PLSCNT does not reach the predetermined value in the step S24, the processing returns to the step S8, in which the writing and erasing operation by the erase setup instruction and the erase instruction is carried out.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Noguchi teaches a method and apparatus for performing erase testing on a semiconductor device. Kobayashi teaches a method and apparatus for testing a plurality of semiconductor memories in parallel. Applicants are invited to read/review additional pertinent prior arts included herein.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 703-305-7755. The examiner may normally be reached Mon – Thur 7:30 am to 4:30 pm and every other Fri 8:00 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 703-305-9595. The fax phone number for the organization where this application is assigned is 703-746-7239.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the receptionist at 703-305-3900.

Mujtaba Chaudry
Art Unit 2133
April 28, 2004

ALBERT DECADY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100